Statistical Ineffective Fault Attacks on Masked AES with Fault Countermeasures

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ASIACRYPT 2018

IAIK - Graz University of Technology

Motivation

Building cryptographic implementations is challenging:

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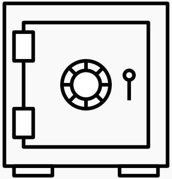
- Requires usage of proper cryptographic primitives



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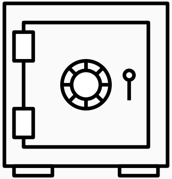
Building cryptographic implementations is challenging:

- Requires usage of proper cryptographic primitives
- But often also the usage of additional defenses ...
  - Microcontroller
  - FPGAs
  - ASICs



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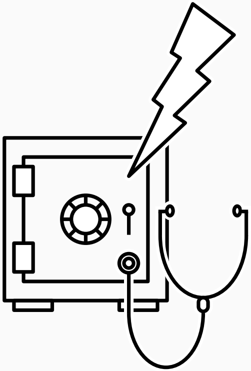
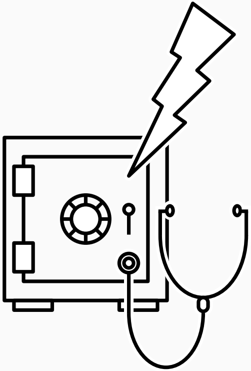
  - Microcontroller
  - FPGAs
  - ASICs
- ... because of implementation attacks



Motivation

- Proper cryptography does not mean practical security



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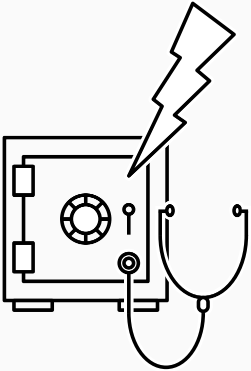

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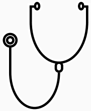
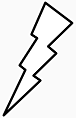
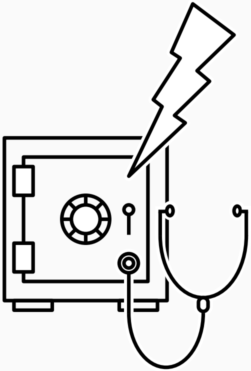
- Secrets can be extracted by:



Power Analysis



Fault Attacks



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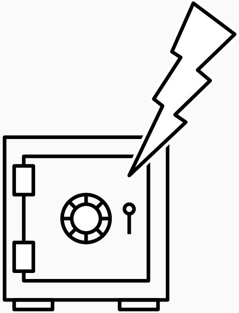

Fault Attacks

- Get physical access to target device:
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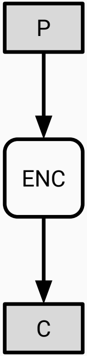

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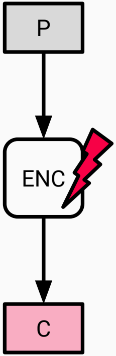

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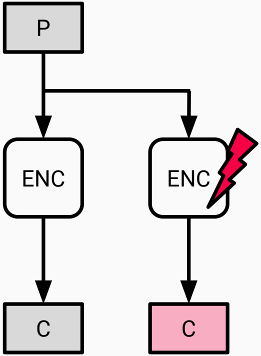

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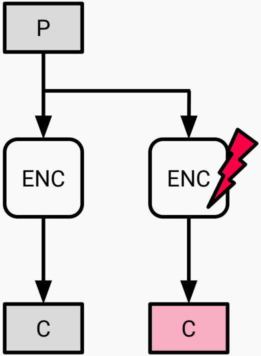

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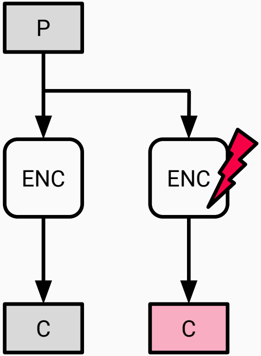
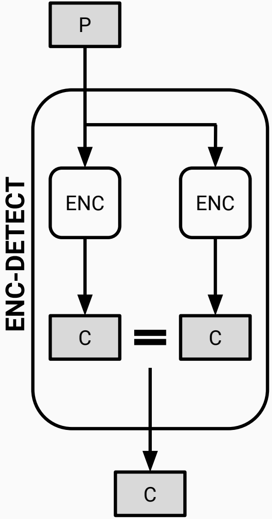
⇒ Differential Fault Attack (DFA)



Fault Countermeasures - Detection

- Use redundancy to detect faults



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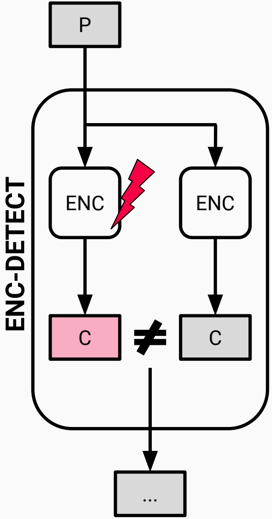

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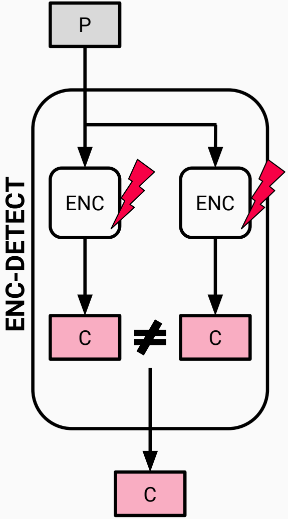

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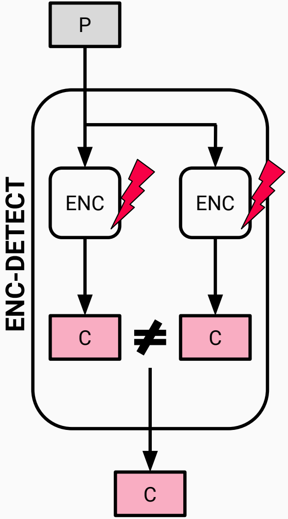
→ More redundancy, Enc-Dec, etc...



Statistical Ineffective Fault Attacks (SIFA)

- We presented SIFA at CHES 2018:
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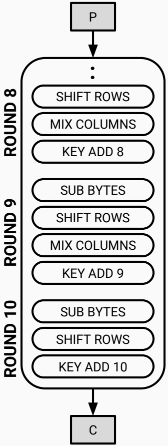
- We demonstrated applicability to AE schemes at SAC 2018
- What about power analysis countermeasures?

SIFA on AES in Pictures



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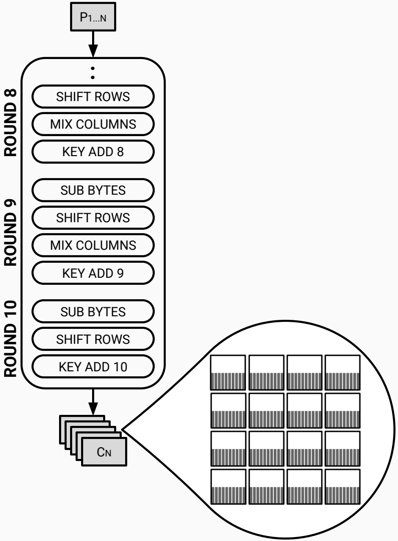

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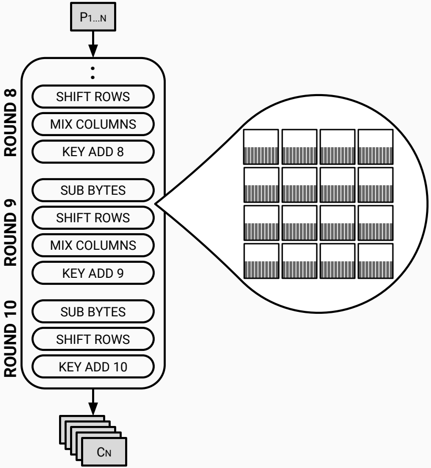

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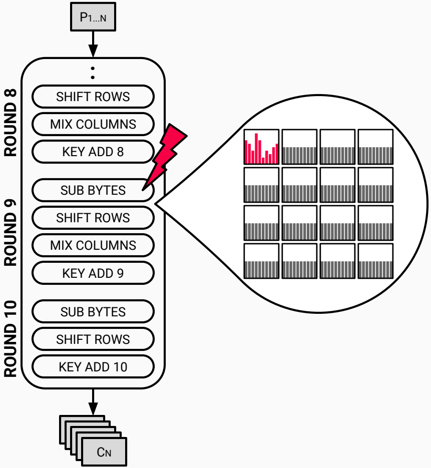

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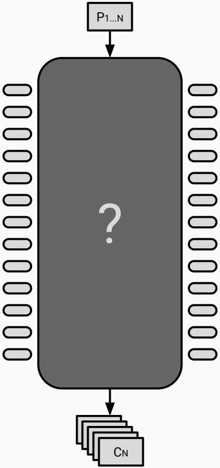

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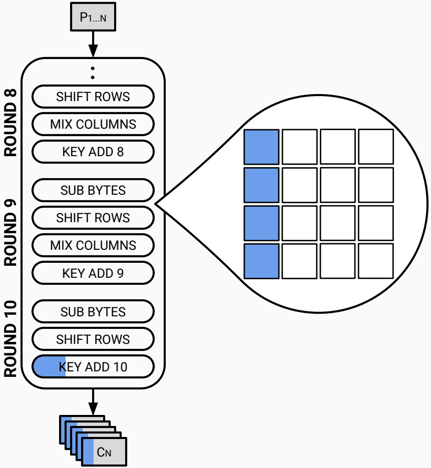

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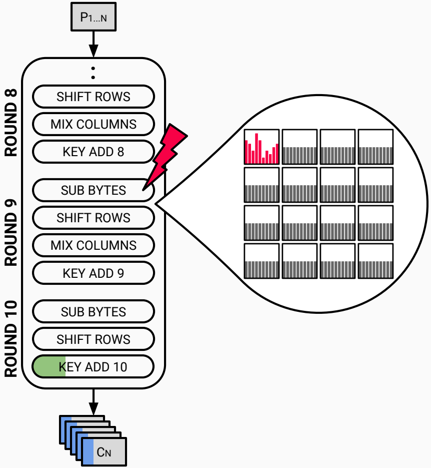

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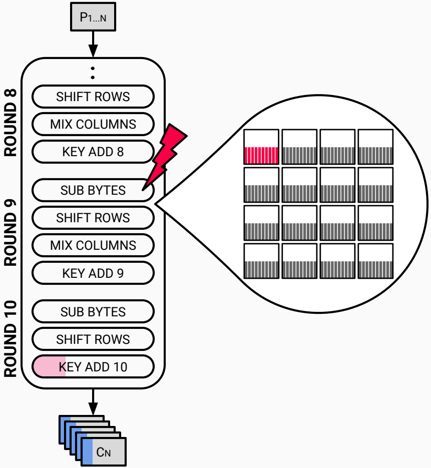

What about fault countermeasures?

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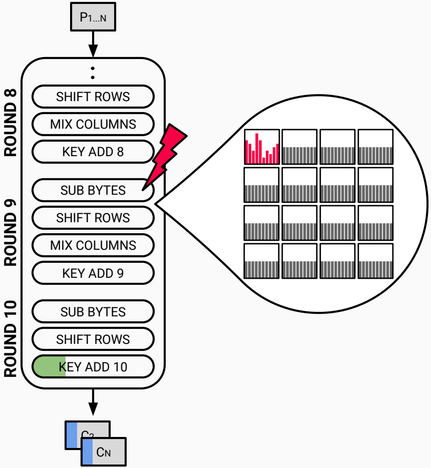
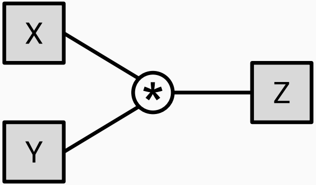


*only correct computations are considered

Ineffective Faults on AND



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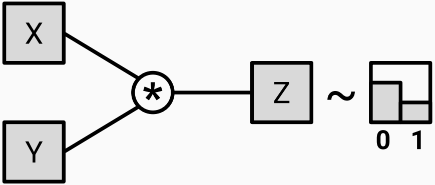

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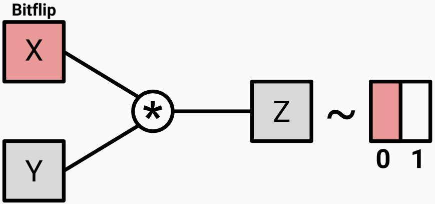

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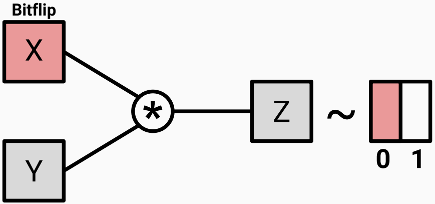
Ineffective Faults on AND

Also works with:

- Other instructions:
  LOAD, STORE, XOR
- Other fault types:
  Random, Stuck-at, Skip



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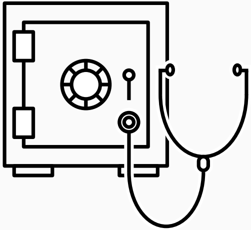

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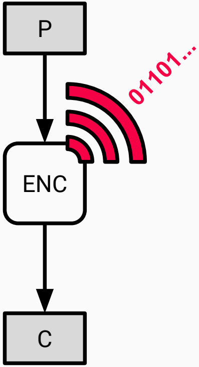
- Circuits leak information via side-channels, e.g. power consumption



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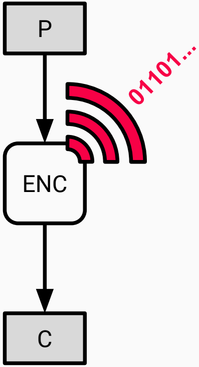

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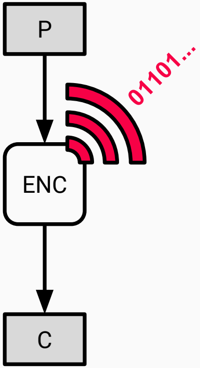

Power Analysis

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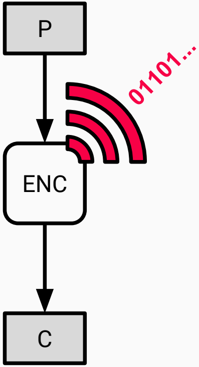
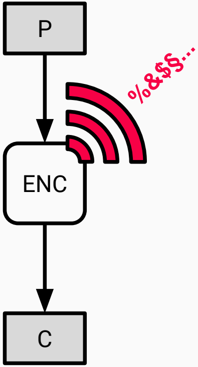
- Correlation between processed data and power consumption
- Problematic if processed data contains secrets



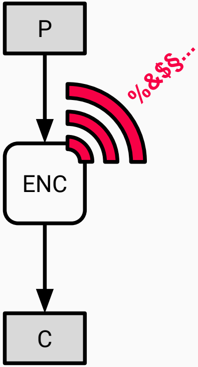
Power Analysis Countermeasures

- Make power consumption independent of processed data
  - Requires hardware support (filters, noise generators)



Power Analysis Countermeasures

- Make power consumption independent of processed data
  - – Requires hardware support (filters, noise generators)
- Make processed data independent of the actual data
  - + "Masking" can be done on algorithmic level



Masking Idea

- Split a value x into multiple “shares” s.t.:
  - The XOR-sum over all x_i equals x
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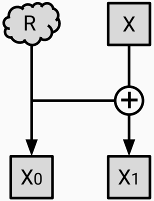

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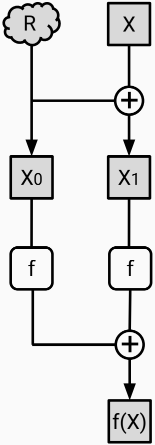

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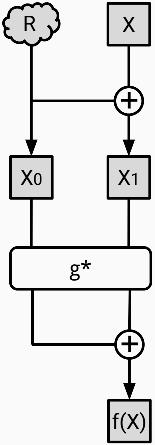

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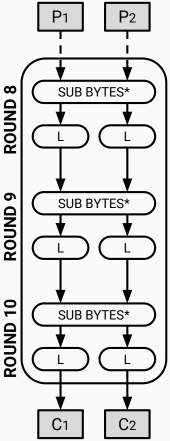
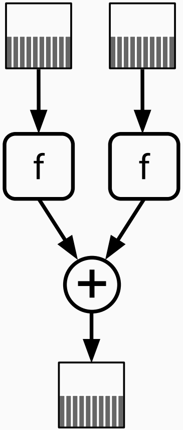
- Applied to AES →



Does our attack still work?

SIFA on Masked AES with Fault CM

- Faulting single shares in linear functions does not work...



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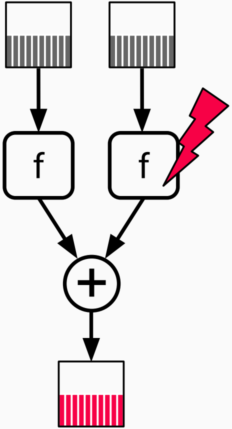

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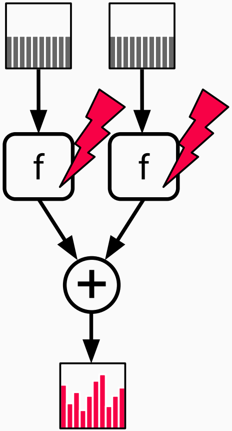

SIFA on Masked AES with Fault CM

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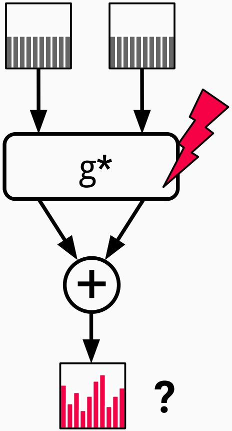
- Faulting all shares would work but is boring...
- Can faulting single shares in non-linear functions lead to a bias in the unshared value?



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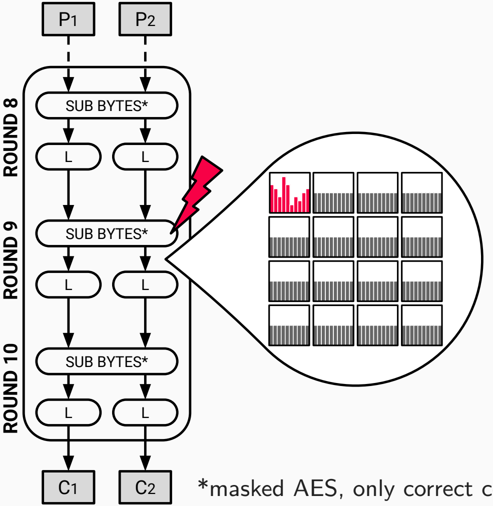

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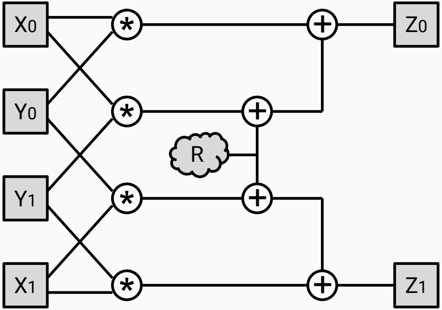
Faults on Masked AND



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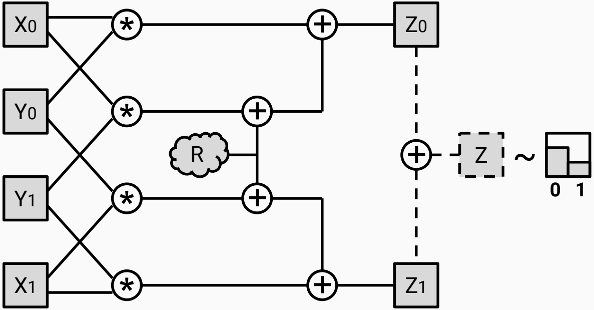

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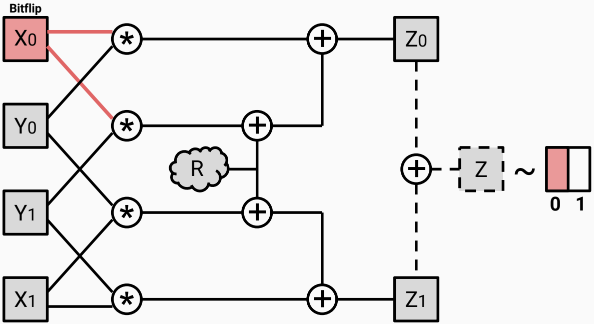

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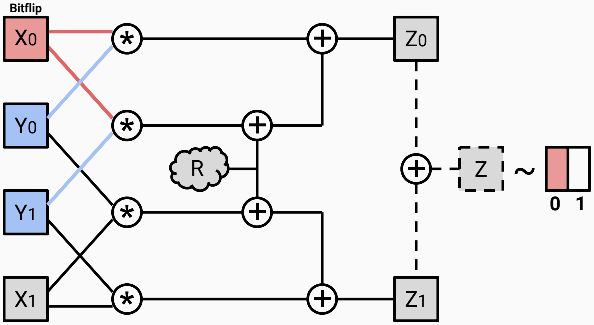

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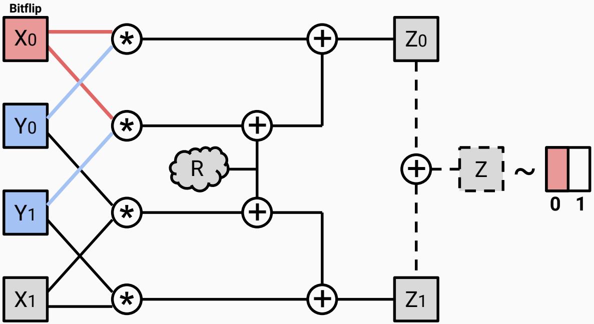
Faults on Masked AND

Also works with:

- Other types of faults
- Higher-order masking
- Threshold Implementations



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Target: First-order masked AES by Schwabe and Stoffelen et al.

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- ARM Cortex M4, ASM optimized

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→ Originally no fault countermeasures, we added "perfect" fault detection

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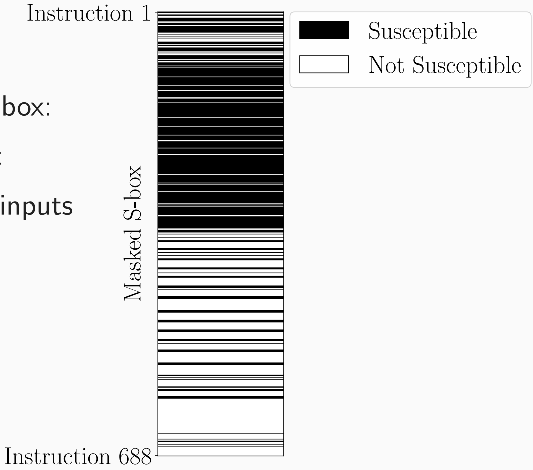

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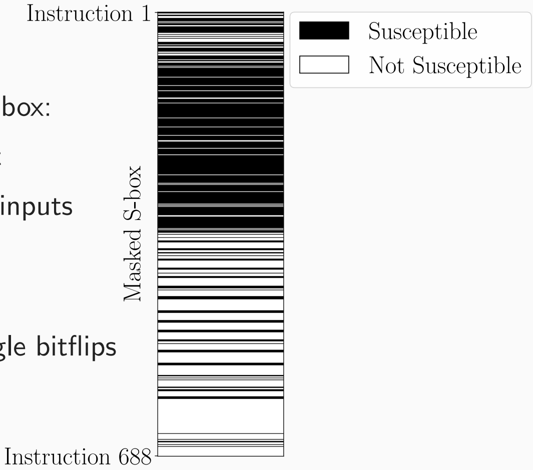
- Check if correct outputs are non-uniform, i.e. if key recovery would work

⇒ 52 % of instruction are "susceptible" to single bitflips

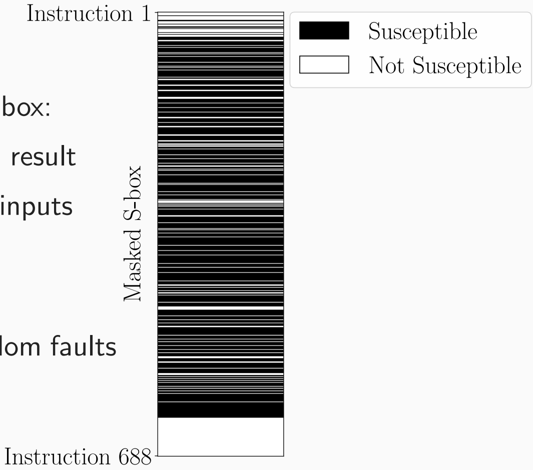


Simulated Faults on Masked AES with Fault Detection

For each individual instruction in the masked Sbox:

- Simulated fault: Randomized 8 bits of the result
- 2000 faulted Sbox computations, random inputs
- Check if correct outputs are non-uniform, i.e. if key recovery would work

⇒ 70 % of instruction are "susceptible" to random faults



Simulated Faults on Masked AES with Fault Detection

Exact numbers for one of the susceptible instructions

Fault Effect	# Ineffective Faults	# Faulted Encryptions	# Recoverable Key Bits
Flip one bit	194	386	32
Set one bit to zero	214	428	32
Randomize one bit	574	763	32
Flip one byte	192	2 940	128
Set one byte to zero	192	3 129	128
Randomize one byte	602	1 808	128
Instruction skip	400	45 527	128

Practical Results

Target: POC higher-order masked AES by Rivain et al.

- Setup: Clock glitches on ATXmega 128D4

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⇒ About 1000 faulted encryptions required

⇒ Thousands of possible fault locations

A word on other countermeasures

- Self Destruction
- Frequent Re-keying
- Multi Party Computation

Summing up

SIFA is quite powerful...

- Works for many ciphers and AE schemes

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- Breaks both fault and power analysis countermeasures
- Attacker does not need to hit specific bits/bytes
- Attacker does not need know how the faults influence the computation

Q?